DESIGN AND ANALYSIS OF LOW POWER CARRY LOOK AHEAD ADDER USING SUBTHRESHOLD ADIABATIC LOGIC

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ABSTRACT

In this work achieves the ultra low power requirement is to operate the digital logic gates in sub threshold region. Adiabatic logic style has emerged as a promising approach to achieve ultra low power and that exchange no energy with the environment and therefore no energy loss in the form of dissipated heat. The signal energies stored in the circuit capacitances are recycled instead of being dissipated as heat. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. This work proposes that SAL- Subthreshold Adiabatic Logic to design the 4-bit basic structure of carry look ahead adder (CLA) with output load capacitance in every logic gates to reduce the heat dissipation. Simulations show that subthreshold adiabatic units can save significant energy compared with a logically equivalent static CMOS implementation. Results are validated through simulations in 45-nm CMOS technology using CADENCE.

Key Words: Adiabatic logic, subthreshold logic, CLA, Ultra low power.

1. INTRODUCTION

A low power VLSI chips become need from such evolution forces of integrated circuits. While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever shrinking size of the integrated circuits. Such high power density introduces reliability concerns such as, electro migration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance. The term “adiabatic” describes the thermodynamic processes in which no energy exchange with the environment, and therefore no dissipated energy loss. Practically supply given by using resonant inductor circuits. Conventional CMOS logic gates used to implement the adders. Dynamic power dissipation is due to charging and discharging(switching0→1,1→0). When switching occurs NMOS and PMOS transistors are conducting current directly from supply to ground. It causes heat dissipation. Adiabatic logic circuits reduce the energy dissipation during switching process, and utilize this energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the ramp type power supply. Here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Hence adiabatic switching technique offers the less energy dissipation and reuses the stored energy in the output load capacitance by reversing the current source. Adiabatic circuits are low power circuits which use “reversible logic” to conserve energy.
2. SUBTHRESHOLD LOGIC

Sub threshold logic operates with the power supply VDD less than the transistors threshold voltage \( V_t \). This is done to ensure that all the transistors are indeed operating in the sub threshold region.

3. PRINCIPLE OF ADIABATIC LOGIC

The word adiabatic comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions that means logic gates are made up of adiabatic logic. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as ENERGY RECOVERY CMOS. Reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems.

4. ADIABATIC GATES

We implemented a SAL-based standard cell library, consisting of common digital gates, such as buffer/inverter, two-input and three-input functions, complex gates, and special gates like half and full adder, which are necessary to implement the 4-bit basic structure of CLA. The digital gates of the library are developed at the transistor level using ramp type supply voltage. These structures resemble either the pull-up or the pull down network of the static conventional logic. For example, to implement a NAND or a NOR gate, simply the pull-up network can be placed between the supply clock and the output load capacitors, whereas an AND or an OR gate can be implemented using the pull-down network.

5. ADIABATIC SWITCHING

Adiabatic switching can be achieved by charging the capacitor from a time varying voltage source or constant current source as shown in Fig.1.1. Here, \( R \) represents the on-resistance of the PMOS network. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuit, thus requires non standard power supplies with time varying voltage, also called pulsed power supplies. Here, the load capacitance is charged by a constant current source (instead of the constant-voltage source as in the conventional CMOS circuits).
6. BASIC STRUCTURE OF CLA

The basic structure of carry look ahead adder is constructed by cascading full adders (FA) blocks in the series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carry out of one stage is fed directly to the carry-in on the next stage.

\[ S_i = A_i \oplus B_i \oplus C_i \]

\[ C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i \]

7. EXISTING METHOD

CONVENTIONAL CMOS LOGIC

In conventional CMOS based basic structure of carry look ahead adder (CLA) implemented by using conventional CMOS and this method uses constant power supply (VDD). Conventional CMOS logic gate used to implement the CLA.

- More no of the transistors so area increased.
- Temperature leakage is high. (i.e) Heat dissipation is increased.
- Power waste is increased.
- The overall performance of the circuit is very low. so weak operation will occur.
- Delay is reduced.
8. PROPOSED METHOD
ADIABATIC LOGIC

To implement SAL-based standard cell library, consisting of common digital gates, such as buffer/ inverter, 2 input and 3 input functions, complex gates are necessary to implement using this adiabatic based gates we can design any digital circuits. Example adders and multipliers. The transistor count will be almost half compared with the conventional CMOS logic design as in SAL basic logic gates have been implemented using either the pull-up or the pull-down transistors. (e.g.) To implement a NAND or a NOR gate, simply the pull-up network can be placed between the supply clock and the output load capacitors.
9. ADVANTAGES

- The transistors count will be almost half compared with the conventional CMOS logic design.
- The SAL technique can be used to make the circuit more energy efficient.
- Area is reduced.
- Delay reduced.
- Reduced heat dissipation.
- Achieved low power so power waste is reduced.

10. APPLICATIONS

- Adiabatic logic is used for the low power CMOS circuits. Adiabatic technique has been effective to power minimization in deep submicron VLSI systems.
- This logic scheme can be used in future energy-saving embedded circuits and mainly for energy efficient devices.
- Subthreshold circuits will suitable for specific applications which required extremely low power consumption (e.g portable electronic devices).

REFERENCES


